

1/f Noise Characterization of Bilayer MoS₂ Field-Effect Transistors on Paper with Inkjet-Printed Contacts and hBN Dielectrics

Lorenzo Pimpolari,* Gabriele Calabrese, Silvia Conti, Robyn Worsley, Subimal Majee, Dmitry K. Polyushkin, Matthias Paur, Cinzia Casiraghi, Thomas Mueller, Giuseppe Iannaccone, Massimo Macucci, and Gianluca Fiori

1/f noise represents the dominant source of noise in the low-frequency range in several physical systems, including field-effect transistors. Its investigation can provide very important information on the fabrication process, highlighting the steps that are more prone to the introduction of defects. Here, 1/f noise in bilayer MoS₂ transistors on paper with inkjet-printed Ag contacts and hBN dielectric is investigated. These devices are promising building blocks for future low-cost, flexible, and easily recyclable disposable electronics. The analysis of 1/f noise, performed following Hooge's empirical approach, results in a Hooge parameter $\approx 1-10$, which is comparable to those reported for bilayer MoS₂ transistors on SiO₂. The present results indicate that the noise properties of the investigated devices are stable against substrate bending and are mainly determined by the printing of the dielectric, while not being sensibly affected by the use of the paper substrate. These results are promising for the further development of low noise 2D material-based flexible electronics on paper.

1. Introduction

In the last few years, there has been an increasing interest toward the development of ubiquitous electronic systems, combining functional features, such as extremely small thickness,^[1] small-weight,^[2] large mechanical flexibility,^[3] wrapping onto

L. Pimpolari, Dr. G. Calabrese, Dr. S. Conti, Prof. G. Iannaccone, Prof. M. Macucci, Prof. G. Fiori
Dipartimento di Ingegneria dell'Informazione
Università di Pisa
Via Girolamo Caruso 16, Pisa 56122, Italy
E-mail: lorenzo.pimpolari@ing.unipi.it

Dr. R. Worsley, Dr. S. Majee, Prof. C. Casiraghi
Department of Chemistry
University of Manchester
Manchester M139PL, UK

Dr. D. K. Polyushkin, Dr. M. Paur, Prof. T. Mueller
Institute of Photonics
Vienna University of Technology
Vienna 1040, Austria

 The ORCID identification number(s) for the author(s) of this article can be found under <https://doi.org/10.1002/aelm.202100283>.

© 2021 The Authors. Advanced Electronic Materials published by Wiley-VCH GmbH. This is an open access article under the terms of the Creative Commons Attribution License, which permits use, distribution and reproduction in any medium, provided the original work is properly cited.

DOI: 10.1002/aelm.202100283

irregular surfaces,^[4] and wearability.^[5] In this context, atomically thin MoS₂ films have attracted particular interest because of chemical robustness and the large availability of the raw material,^[6] and have been exploited as channel layer in flexible field-effect transistors (FETs) on polyimide,^[7-10] polyethylene terephthalate,^[11-14] polyethylene naphthalate,^[15] and polydimethylsiloxane substrates.^[16]

The continuous increase in the demand of low-cost and disposable electronic systems, also motivated by emerging Internet of Things (IoT) applications, has raised important concerns regarding sustainability, such as the treatment of waste at the end of the product life-cycle.^[17] Paper-based consumer electronics offers a simple solution to this issue by combining

an environmentally friendly material and simple recycling, with a very low cost and large area flexible substrate.^[18] These properties make paper an extremely promising substrate for electronic applications in the “More Than Moore” context, toward a functional diversification of electronic systems, as recently also outlined by the “International Roadmap for Devices and Systems.”^[19] MoS₂-based FETs on paper were first obtained by means of hydrothermal synthesis.^[20] More recently, the present authors demonstrated low-voltage and transfer printed MoS₂ FETs on paper in a channel array configuration, with inkjet-printed hexagonal boron nitride (hBN) gate dielectric and Ag contacts.^[21] These flexible devices exhibited good performance with average carrier mobility of 5.5 cm² V⁻¹ s⁻¹ (maximum of 25 cm² V⁻¹ s⁻¹) and on-off current ratio of $\approx 10^4$ over a statistics of 26 devices, and have been successfully used in digital and analog applications, such as high-gain inverters, AND gates, and current mirrors.^[21]

In these applications, as well as in sensors and transducer systems often operating at low signal levels, low-frequency noise (LFN, or 1/f noise, where f is the frequency) is a crucial performance metric.^[22,23] In addition, the reduced dimensionality of atomically thin MoS₂ films makes them extremely sensitive to the surface and interface conditions, further increasing the importance of 1/f noise in electronic devices based on this material. LFN has been extensively investigated in mechanically exfoliated single layer,^[24] few layer,^[25,26] and multilayer,^[26] as well as chemical vapor deposition (CVD)-grown single layer^[27]

and few layer^[28] MoS₂ FETs prepared on rigid substrates such as SiO₂ and Al₂O₃. These results indicate that the noise properties of MoS₂ FETs critically depend on material quality and improve with increasing channel thickness, approaching those of graphene for relatively thick films (15–18 layers).^[26] Recently, Kaushik and collaborators demonstrated a significant increase in $1/f$ noise in suspended MoS₂ FETs as compared to similar devices on SiO₂, a result attributed to the larger area exposed to ambient conditions in the suspended configuration.^[29] Encapsulation of MoS₂ FETs in Polyethylene (PE) resulted in degraded noise performance with respect to bare devices, as a consequence of the introduction of a large number of traps at the PE/MoS₂ interface.^[30] On the other hand, noise reduction was observed exploiting an Al₂O₃ high-*k* passivation layer deposited by means of atomic layer deposition, a highly controllable deposition technique.^[31] Despite these extensive studies, LFN characterization of a 2D material-based FET on a flexible substrate, which is of high relevance for flexible electronics and optoelectronics applications, has never been reported.

Here, we investigate LFN in printed MoS₂ FETs on paper, exploiting a CVD-grown and later transferred MoS₂ channel, inkjet-printed hBN gate dielectric and Ag contacts. These devices could represent important building blocks for future flexible and easily recyclable electronic systems, provided that their electronic properties are comparable to those of analogue devices prepared using conventional fabrication techniques and are not degraded by substrate bending. Since this technology is still at an embryonic stage, insights into the main physical effects that could be detrimental for device performance (e.g., the presence of defects) are needed. From this point of view, LFN analysis can shed light on the processing steps that are more prone to the introduction of defects and can provide useful guidelines toward the achievement of high-performance devices. In this work, we present the first LFN investigation for a 2D material-based FET with inkjet-printed components and, more in general, for a FET on paper, which represents an important step toward low-cost and distributed electronics on a flexible, and easily recyclable substrate. Obtained results show that the noise properties of fabricated devices are comparable to those reported for analogue devices prepared on rigid substrates using standard microfabrication techniques, hence holding great promise for low-noise electronics based on 2D materials on paper.

2. Results and Discussion

MoS₂ is grown by CVD on a 13 × 13 mm² Al₂O₃(0001) substrate. After growth, MoS₂ is patterned into parallel stripes that will form the device channels (Figure 1a). MoS₂ patterning facilitates the following fabrication of FETs as well as the eventual creation of interconnections and circuits.^[21] The atomic force microscopy image shown in Figure 1b, taken in the central zone of the substrate, shows that the MoS₂ film is homogeneous in thickness, with a very high area coverage of 98.5%, as determined with the help of the open-source software ImageJ^[32] and in agreement with results presented in a previous article.^[21] Figure 1c shows a Raman spectrum of the MoS₂ film taken at substrate center. The characteristic E_{2g}¹–A_{1g}

spacing of 21.2 cm⁻² reveals that the MoS₂ film is bilayer. After patterning, the MoS₂ stripes are transferred onto the paper substrate via a transfer printing technique [see (i) in Figure 1d]. Further details on the MoS₂ growth and transfer procedure are reported in a previous paper.^[21] Figure 1d shows a schematic diagram of the FET fabrication sequence, which starts with (ii) inkjet-printing of the Ag source and drain contacts, followed by (iii) inkjet-printing of the hBN gate dielectric on the source and drain contacts as well as on the MoS₂ channel. The hBN film is printed starting from custom-made aqueous solution, whose preparation details, as well as morphological and electrical characterizations, have been reported elsewhere.^[33,34] Finally, to conclude the FET fabrication process, the Ag gate contact is inkjet-printed on top of the hBN film (iv). Both the metallic contacts as well as the dielectric film are inkjet-printed using a Fujifilm Dimatix Materials Printer 2850. The Ag contact is printed using a 1 pL nominal volume cartridge, while hBN is printed using a 10 pL nominal volume cartridge. A total of 9 FETs are fabricated and investigated in this study. These devices have channel length (*L*) ranging from 20 to 40 μm, and width (*W*) ranging from 30 to 150 μm, respectively.

An optical micrograph of a representative MoS₂ FET on paper is shown in Figure 2a. The corresponding schematic layout is reported in Figure 2b, showing the FET structure, layer sequence, and the bias voltages applied during electrical characterization. The gate-source voltage (*V*_{GS}) and drain-source voltage (*V*_{DS}) are applied to the gate and drain contacts, respectively, the source contact is connected to ground. All measurements are carried out under ambient conditions and at room temperature. The bias voltages for both DC and noise measurements are supplied with a Keithley 4200A-SCS Parameter Analyzer. For the noise measurements, the channel current fluctuations are amplified with a low-noise amplifier and their spectrum is measured with a SR785 Dynamic Signal Analyzer. Further details on the measurement setup are available in Section S2 (Supporting Information).

The transfer characteristic of one representative FET is reported in Figure 2c for *V*_{DS} = 2 V. The threshold voltage (*V*_{th}) extracted in the linear regime is ≈ -1 V. Small variations in *V*_{th} are observed among the fabricated FETs, and for all devices *V*_{th} is found to be in the range -1 to 1 V. The output characteristics of the same device whose transfer characteristic is shown in Figure 2c are reported in Figure 2d. These curves show the presence of a Schottky barrier for low *V*_{DS} when *V*_{GS} < 2 V, while for larger *V*_{GS} a linear dependence between the channel current (*I*_{DS}) and *V*_{DS} is visible, suggesting the presence of an ohmic contact. Formation of ohmic contacts is attributed to the bending of the MoS₂ conduction band with increasing *V*_{GS}, which promotes charge injection from the contacts into the channel. Further details on the nature of the Ag/MoS₂ contacts can be found in Section S1 (Supporting Information).

Electrical noise in FETs is a complex phenomenon, which not only depends on defects or trap states within the semiconductor itself, but can also be influenced by defects located at the semiconductor/substrate as well as the semiconductor/dielectric interfaces.^[35] In order to distinguish the contributions of the different potential noise sources, we carried out a step-by-step fabrication of a typically investigated FET, followed by LFN characterization after each fabrication step. In

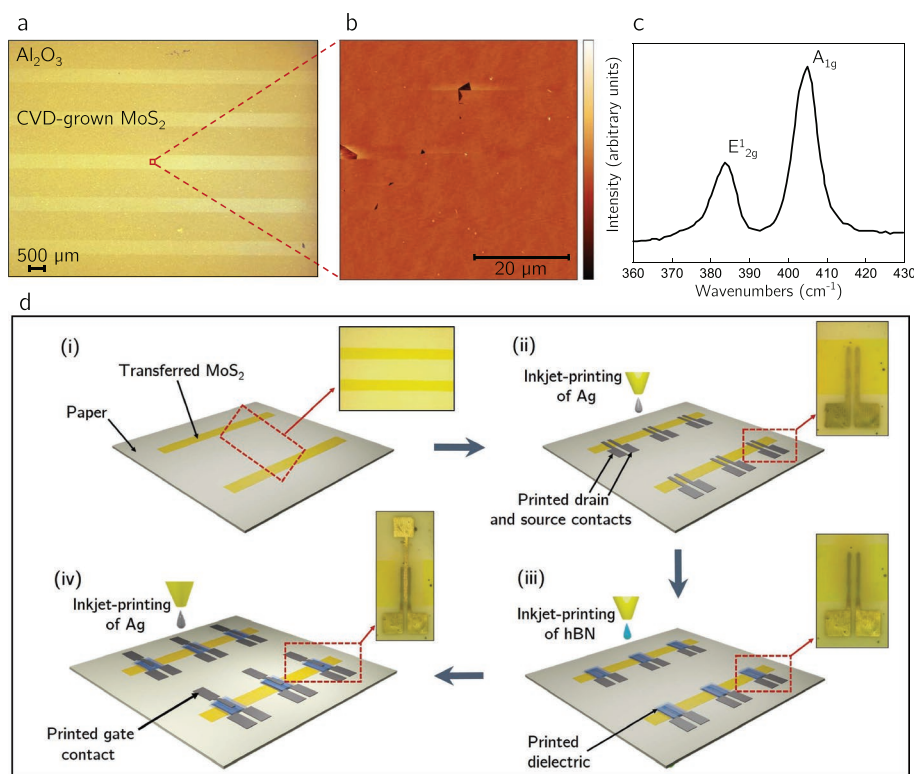


Figure 1. Characterization of CVD-grown MoS₂ and FETs fabrication. a) Optical micrograph of the MoS₂ stripes on the native Al₂O₃(0001) substrate. b) 50 × 50 μm² atomic force micrograph of the as-grown MoS₂ film on the native substrate, taken at substrate center. The scale bar ranges from 0 to 4 nm. c) Raman spectrum of the MoS₂ film, taken in the center of the sample. d) Schematic diagram showing the used fabrication sequence for the realization of MoS₂ FETs on paper. At first, the MoS₂ stripes are transfer-printed on paper (i). Successively, the drain and source contacts (ii), the hBN dielectric (iii), and, finally, the top gate contact (iv) are deposited by means of inkjet-printing. The insets show optical micrographs corresponding to the different fabrication steps.

particular, LFN characterization is performed for the three different steps: i) after the inkjet-printing of the Ag source and drain contacts on MoS₂, ii) after inkjet-printing of the hBN gate dielectric, and iii) after inkjet-printing of the Ag top gate contact (i.e., in a FET structure). The step-by-step fabrication and characterization procedure allows us to investigate LFN both when the MoS₂ film is exposed to air (Figure 3a, red box), and when it is covered with the hBN gate dielectric (Figure 3a, blue box).

Figure 3b shows I_{DS} as a function of V_{DS} , both before and after inkjet-printing of the hBN gate dielectric. After inkjet-printing of the hBN film, an increase in the conductivity of the channel is observed. Indeed, the channel resistance R_{ch} is reduced from 2.96 to 1.82 MΩ after the dielectric deposition. The increased channel conductivity is likely related to doping of the MoS₂ active film from the chemicals composing the hBN ink, in analogy to what previously observed in inkjet-printed graphene films.^[36] This hypothesis is compatible with the shift of V_{th} toward smaller values observed in the transfer characteristics of back-gated MoS₂ FETs fabricated on SiO₂/Si, collected prior and after the hBN deposition (see Figure S3 in the Supporting Information). The observed decrease in V_{th} indicates the introduction of n-type doping within the MoS₂ film during hBN printing, which is the expected type of doping from the chemicals in the ink.^[36]

The I_{DS} - V_{DS} characteristics reported in Figure 3b indicate the presence of a Schottky-type contact at the different fabrication steps (in agreement with the data reported in Figure 2d), as a consequence of Fermi level pinning at the metal/MoS₂ interfaces.^[37–39]

The power spectral density (PSD) of I_{DS} , $S_{I_{DS}}$, normalized to the square of I_{DS} is reported in Figure 3c as a function of f , in the low-frequency range between 1 and 200 Hz. The collected spectra are measured for $V_{DS} = 30$ V, corresponding to the region where the current–voltage characteristics have a linear behavior, in order to minimize the contribution of contact resistance to the noise spectra. According to the empirical Hooge law, the LFN PSD can be expressed as^[40]

$$\frac{S_{I_{DS}}}{I_{DS}^2} = A \frac{1}{f^\gamma} \quad (1)$$

where A is the noise amplitude, while β is the exponent of I_{DS} and γ is the exponent of f (which are ideally equal to 2 and 1, respectively, in the case of flicker noise^[35]). The spectra reported in Figure 3c reveal that the PSD, both prior and after hBN deposition, has a $1/f$ behavior, i.e., γ is close to 1, thus confirming that flicker noise is dominating the noise spectrum in the low-frequency range. Further considerations on γ will be discussed in the following. After printing the hBN film,

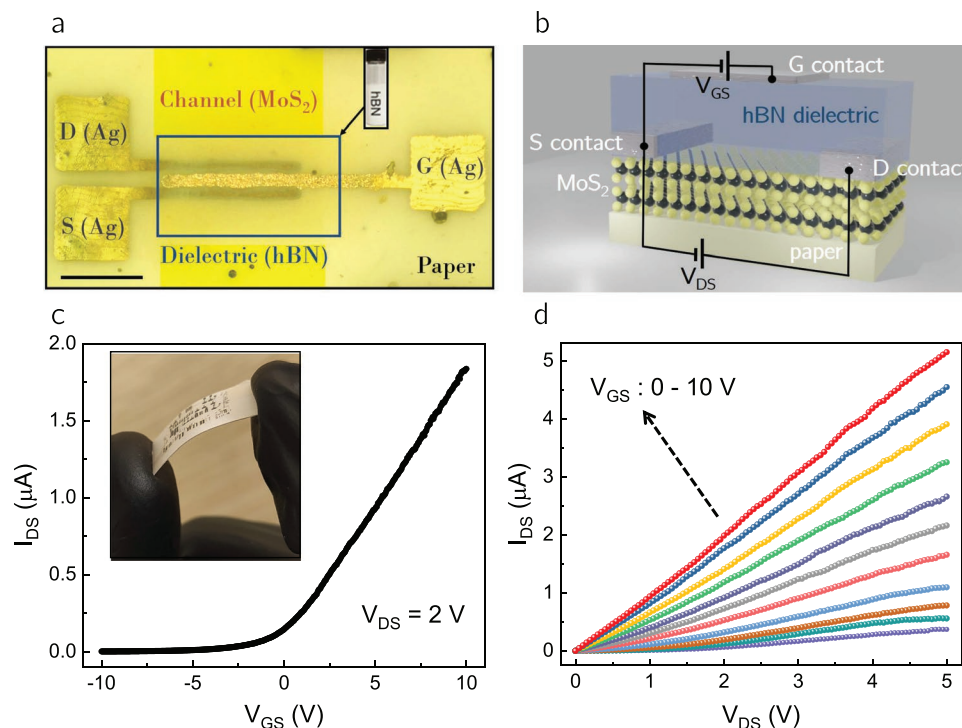


Figure 2. Electrical characterization of MoS₂ FETs on paper. a) Optical micrograph showing an individual MoS₂ FET on paper. The scale bar corresponds to 250 μm. In the inset, a vial containing the hBN ink used to inkjet-print the gate dielectric is shown. b) Schematic diagram of the FET structure, showing its layer sequence and biasing voltages. c) Transfer characteristic of one of the fabricated FETs, measured for V_{DS} = 2 V. In the inset, an optical micrograph showing arrays of MoS₂ FETs fabricated on the paper substrate are reported. d) Output characteristics of the same FET whose transfer characteristic is shown in c). The step in V_{GS} equals 1 V.

the measured PSD is found to increase by about one order of magnitude, as compared to the value recorded for bare MoS₂. A comparable behavior has also been observed for all other measured devices (see Figure S4 in the Supporting Information), suggesting that inkjet-printing of hBN introduces defects and trap states at the interface with MoS₂, similarly to what previously reported for PE-passivated MoS₂ FETs.^[30] The significant increase in noise level after printing of hBN indicates that, from the noise point of view, this is the most critical fabrication step for the proposed FETs. This result is

not surprising when considering the fact that the hBN flakes inkjet-printed on MoS₂ present a broad orientational distribution and chemical residuals.

After evaluating how the hBN gate dielectric contributes to the noise level in two-terminal devices, the 1/f noise is investigated in MoS₂ FETs. The PSD as a function of *f* is reported in **Figure 4a**, for the same FET whose transfer and output characteristics are shown in **Figure 2c,d**, for V_{GS} = 8 V and V_{DS} ranging from 250 mV to 5 V. Under these conditions, the FET is operating in the linear regime (i.e., V_{DS} < V_{GS} - V_{th}). Also in this

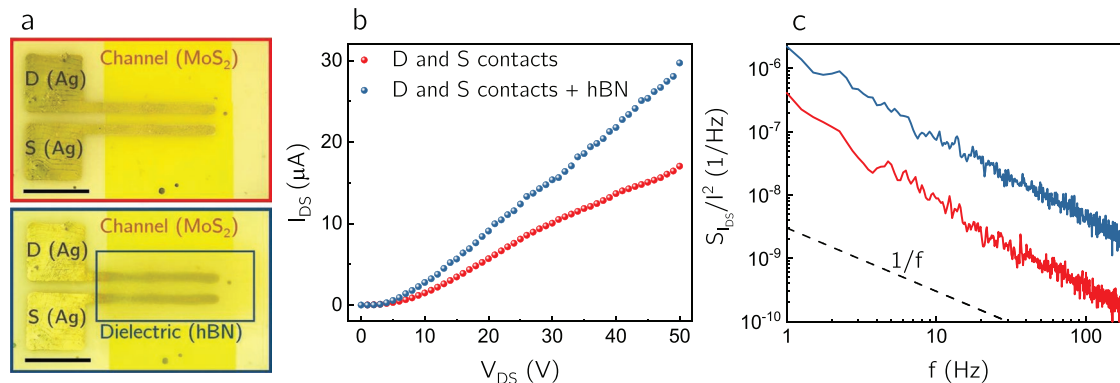


Figure 3. Optical micrographs of 2 contact MoS₂ devices and their electrical characterization. a) Optical micrographs showing the investigated device prior (top, red box) and after (bottom, blue box) hBN printing. The scale bars correspond to 250 μm. b) Current–voltage characteristic and c) normalized PSD of the shown two-contact MoS₂ device taken prior and after hBN deposition. The ideal 1/f slope is reported in c) as a reference.

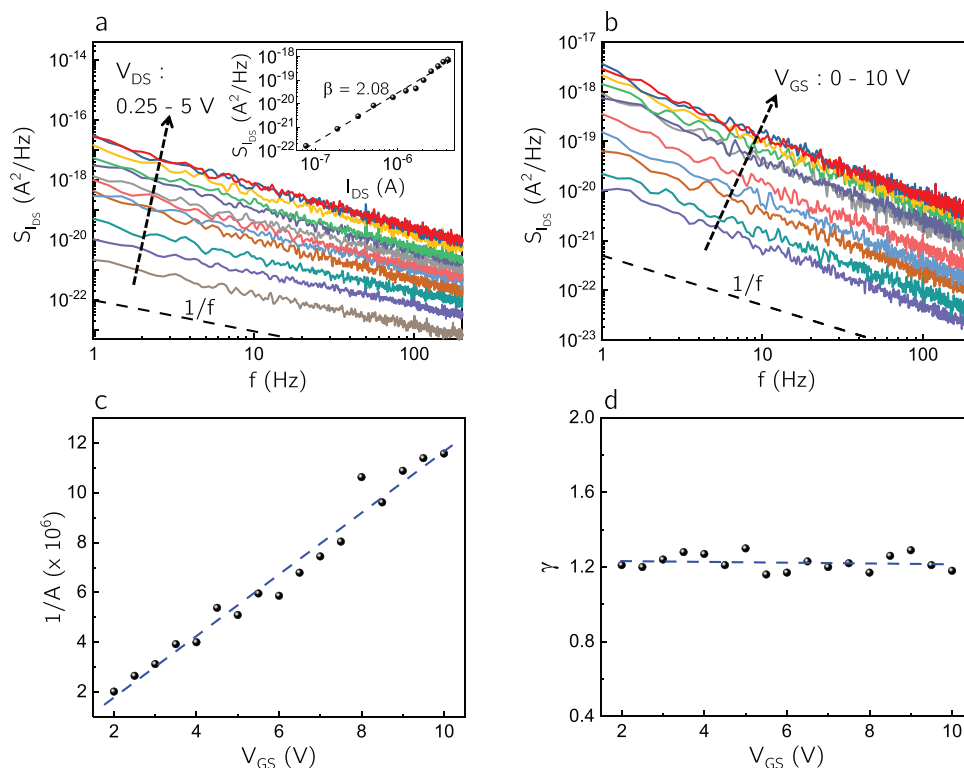


Figure 4. LFN characterization of MoS₂ FETs on paper. a) PSD for the device whose transfer and output characteristics are reported in Figure 2c,d, respectively, measured for V_{DS} ranging from 0.25 to 5 V. The inset shows the dependence of $S_{b_{ps}}$ on I_{DS} . b) PSD measured for V_{GS} between 0 and 10 V (step of 1 V) and $V_{DS} = 2$ V. As a reference, the ideal $1/f$ slope is reported both in a) and b). c) $1/A$ as a function of V_{GS} . A linear fit to the experimental data is shown as a dashed line. d) γ as a function of V_{GS} . The blue dashed line is a guide to the eyes. All measurements reported in a–d) are taken on the same device.

case, for all the studied bias conditions the $1/f$ noise is found to be the dominant source of noise in the investigated frequency range, and no corner frequency to white noise is observed. The inset of Figure 4a shows a log–log plot of $S_{b_{ps}}$ as a function of I_{DS} for the same device. The linear fit to the experimental data returns a value of $\beta = 2.08$, thus confirming the presence of an ohmic contact between the inkjet-printed Ag contacts and the MoS₂ channel at the considered V_{GS} . For few investigated FETs, a value of β smaller than 2 is extracted for the same bias conditions, which might indicate the presence of contact noise introduced by non-ohmic contacts in these devices.^[24] Further details on contact noise in the investigated MoS₂ FETs are available in Section S5 (Supporting Information).

Figure 4b shows the PSD of the FET under investigation collected for different values of V_{GS} , ranging from 0 to 10 V. For all measurements, V_{GS} is larger than V_{th} and $1/f$ noise dominates the noise spectra. The Hooge formula [Equation (1)] can be rewritten as

$$\frac{S_{I_{DS}}}{I_{DS}^2} = \frac{\alpha_H}{N} \frac{1}{f} \quad (2)$$

where α_H is the Hooge parameter, and N is the total number of carriers in the channel (β and γ are approximated to 2 and 1, respectively). In the linear regime, N can be approximated as $N \approx (V_{GS} - V_{th})LWC_G/q$, where C_G is the gate capacitance

per unit area, and q the elementary electric charge. Therefore $1/A$ is expected to be proportional to V_{GS} , which is confirmed by the experimental data reported in Figure 4c, extracted from the results in Figure 4b. In Figure 4d, we report the value of γ as a function of V_{GS} (again from the results of Figure 4b): it is almost constant, with an average value of 1.2, very close to the ideal value of 1. The linear dependence between $1/A$ and V_{GS} that we observed in our bilayer MoS₂ FETs on paper was also reported in previous articles on mechanically exfoliated^[24] and CVD-grown^[41] monolayer MoS₂. On the other hand, a superlinear or quadratic relationship between these quantities was observed in other publications,^[25,27,30,31] suggesting that the fabrication methods, the nature and density of crystallographic defects, as well as the measurement conditions have a strong impact on experimental results for flicker noise in MoS₂ FETs.

Hooge's parameter α_H is independent on device area, and hence can be used as a figure of merit for a direct comparison with previous results reported in the literature. For the device reported in Figure 5a, we extracted $\alpha_H = 1.4$, and for all investigated devices α_H ranges from 1.1 to 11.4 (with an average value of ≈ 5), as shown in Figure 5b. These values are comparable to those previously reported for mechanically exfoliated^[24] and CVD-grown monolayer MoS₂ with grain boundaries on SiO₂/Si measured under ambient conditions,^[42] as well as for CVD-grown monolayer MoS₂-FETs with Ti/Au contacts measured in

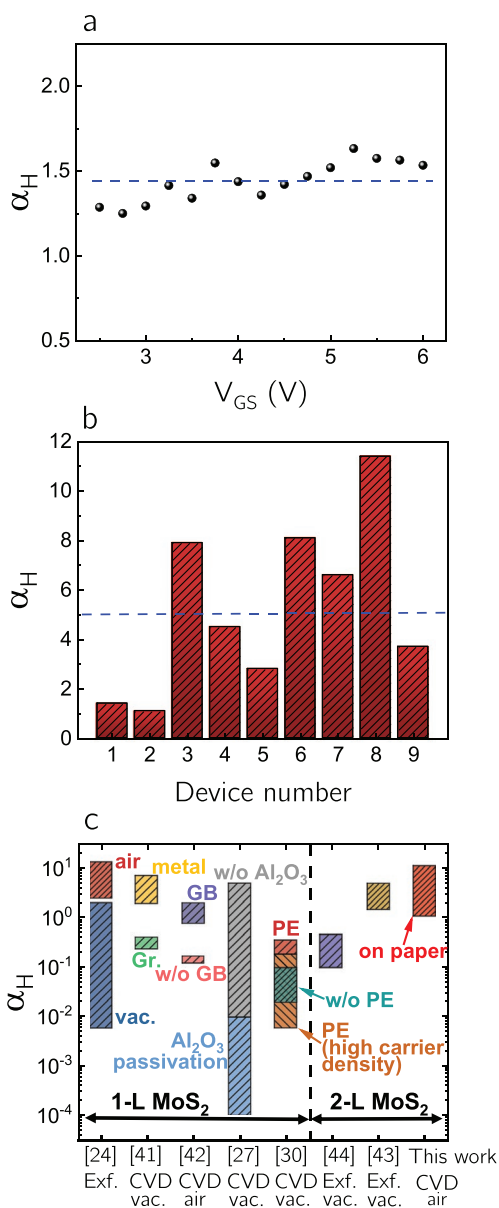


Figure 5. a) α_H as a function of V_{GS} for a representative MoS₂ FET on paper. b) Extracted α_H for the 9 devices investigated in this work. The blue dashed lines in a) and b) indicate the average α_H values. c) Comparison of the values of α_H obtained in this work with previously reported values for CDV-grown and exfoliated monolayer (1-L) and bilayer (2-L) MoS₂ FETs on SiO₂/Si exploiting evaporated contacts (except ref. [41] where graphene contacts are used). Legend: Exf.: mechanically exfoliated MoS₂, CVD: CVD-grown MoS₂, vac.: measured in vacuum, air: measured in air, metal: with metal contacts, Gr: with graphene contacts, GB: with grain boundary, w/o GB: without GB, w/o Al₂O₃: without Al₂O₃ passivation, PE: with polyethylene, w/o PE: without polyethylene.

vacuum.^[41] Remarkably, the obtained values of α_H are also comparable to those found for mechanically exfoliated bilayer MoS₂ on SiO₂/Si exploiting evaporated Cr/Au contacts and measured under ambient conditions.^[43] Smaller values of α_H were previously reported for mechanically exfoliated monolayer^[24] and bilayer^[44] MoS₂ on SiO₂/Si measured in vacuum, due to removal of atmospheric adsorbates/surface contaminants

under vacuum conditions. A comparison of the values of α_H obtained in this work with those reported in the literature for both monolayer and bilayer MoS₂ FETs prepared by CVD and mechanical exfoliation is shown in Figure 5c. Despite the use of a rough and porous substrate such as paper and of inkjet-printed contacts and dielectric layer, the noise properties of our FETs are in line with those reported in the literature for comparable devices prepared using standard techniques and investigated under similar experimental conditions. The obtained results point out that the noise properties of bilayer MoS₂ are not sensibly affected either by film patterning, transfer, and integration on a flexible paper substrate, or by the use of inkjet-printed Ag contacts. Noise measurements are therefore useful to identify methods to optimize the hBN/MoS₂ interface, for example by postfabrication thermal treatments, by exploitation of a high-*k* passivation layer,^[27,31] or by increasing the thickness of the MoS₂ film in order to take advantage of the stronger screening capability of thicker films.^[26,43,45] Further details on the influence of thickness are available in Section S6 (Supporting Information).

The data reported in Figure 5 highlight a device-to-device variation in the measured noise of about one order of magnitude, which, as demonstrated by the measurements reported in Figure S4 (Supporting Information), is mainly due to non-idealities of the MoS₂ film itself, and not to the printed hBN dielectric. This is not surprising considering that the investigated devices are fabricated in random positions of a cm-scale MoS₂ film which, for its intrinsic nature, exhibits small inhomogeneities caused by flux and temperature gradients across the substrate during growth. Remarkably, the observed noise variation is comparable to or even smaller than that observed in both mechanically exfoliated^[24,27] and CVD-grown^[30] single-flake MoS₂-FETs fabricated on SiO₂.

LFN measurements can also be used as powerful tools to investigate the electromechanical properties of the proposed devices. Indeed, the comparison between the power spectral densities measured with and without mechanical strain applied to the device, can provide useful information on whether and how much the electric transport of the device is affected by the applied stress, which is of crucial importance for flexible and wearable electronic applications.^[46]

The mechanical measurements are carried out by measuring the PSD of the channel current applying both tensile and compressive strain to the investigated device by bending the substrate around rigid jigs with different radii, down to 12 mm. The graphs in Figure 6a show the normalized power spectral densities of the channel current collected without the application of mechanical stress (red curve), with the application of tensile strain using a bending radius of 12 mm (blue curve), and again in nonbending conditions, after removal of the applied stress (green curve). The same considerations are valid for the graph of Figure 6b, but in this last case a compressive strain is applied. In both cases there are no major changes in the measured power spectra under the investigated strain conditions. This suggests that the applied mechanical stresses do not introduce delamination of the channel or an increase in the density of defects or traps, and constitutes a promising result in the context of flexible and wearable applications.

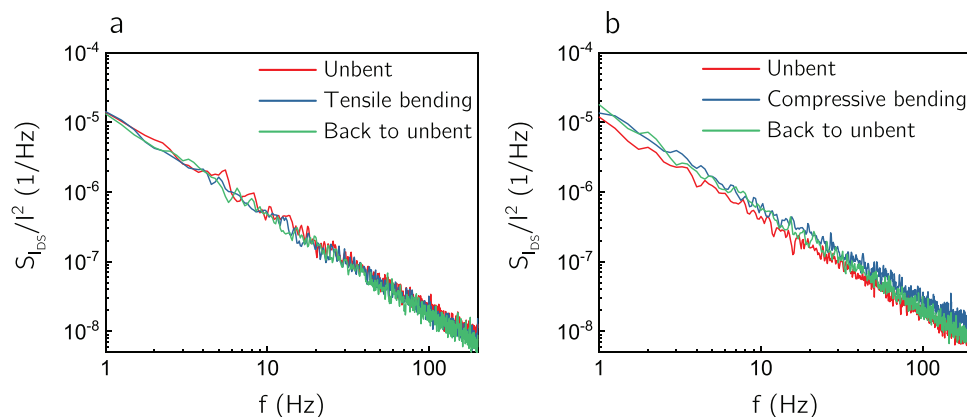


Figure 6. Comparison of LFN measurements with and without applied mechanical stress. a,b) Normalized PSD of a representative device measured without and with the application of a) tensile/b) compressive strain. The bending radius is 12 mm; the bias conditions are $V_{DS} = 1$ V and $V_{GS} = 2$ V.

3. Conclusion

To summarize and conclude, we have investigated $1/f$ noise in bilayer MoS₂ FETs on paper, exploiting inkjet-printed hBN gate dielectric and Ag contacts, which represent promising building blocks for a wealth of IoT applications on a flexible, large area, low-cost, and easily recyclable substrate. $1/f$ noise analysis revealed that inkjet-printing of hBN increases the noise level in two-contact MoS₂ devices by about one order of magnitude, hence representing the device fabrication step that mostly affect the noise properties. The extracted Hooge parameter is in the range of 1.1–11.4, which is comparable to values previously reported for bilayer MoS₂ FETs on SiO₂ with evaporated metal contacts. This observation indicates that the noise properties of bilayer MoS₂ FETs are not degraded by device integration on paper or by the use of inkjet-printed Ag contacts, in agreement with the values of mobility and on-off current ratio, which are also comparable between the two technologies. Measurements carried out under the application of mechanical stress have shown that the fabricated devices are stable against substrate bending and their noise level is not affected by the applied tensile or compressive strain down to a curvature radius of 12 mm. Present results are promising for the further development of 2D material-based paper electronics for a broad range of applications that require low noise levels, such as analog front-end for sensors, an application of growing interest in the IoT context.

4. Experimental Section

Growth, Characterization, and Transfer of MoS₂: Bilayer MoS₂ is grown by CVD on a 13×13 mm² Al₂O₃(0001) substrate. CVD growth is performed at atmospheric pressure using ultrahigh-purity Ar as the carrier gas, following the procedure reported in a previous paper.^[21] The grown film has been characterized by atomic force microscopy (using a Veeco NanoMan vs atomic force microscope), in semicontact mode at ambient conditions, and Raman spectroscopy, with illumination at 532 nm [the output signal has been measured using a spectrometer Horiba iHR320, with a grating with 1800 grooves mm⁻¹ and a liquid nitrogen cooled CCD detection system (Symphony II)]. These characterizations revealed that the film is homogeneous in thickness with an area coverage of 98.5%, and is bilayer. After growth, the MoS₂

film is patterned by means of Ar/SF₆ plasma etching and transferred to the target paper substrate (PEL P60, purchased from Printed Electronics Limited) following the procedures reported in a previous work.^[21]

Device Fabrication: MoS₂ transistors were fabricated in a top-gate configuration using the transferred MoS₂ stripes as channel material. The metal contacts and the gate dielectric were inkjet-printing using a Fujifilm Dimatix Materials Printer 2850. A commercial silver ink (purchased from Sigma-Aldrich) was used to print the contacts, while for the gate dielectric a custom-made hexagonal boron nitride (hBN) ink with a concentration ≈ 2 mg mL⁻¹ was employed. The Ag contacts were printed using a 1 pL nominal volume cartridge, while hBN was printed using a 10 pL nominal volume cartridge. All films were printed at room temperature with a drop spacing of 20 μ m.

Electrical and Noise Characterization: For both electrical and noise measurements the bias voltages were supplied using a Keithley 4200A-SCS Parameter Analyzer. For the noise measurements, the channel current fluctuations were amplified with a low-noise amplifier (based on the integrated circuit LT1793) and the corresponding noise spectra were collected with a SR785 Dynamic Signal Analyzer in the frequency range from 1 to 200 Hz, with a line width of 250 mHz and 800 FFT points. Further details on the measurement setup are available in Section S2 (Supporting Information). All measurements were carried out under ambient conditions and at room temperature.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

L.P. and G.C. contributed equally to this work. The authors acknowledge the ERC PEP2D (Contract No. 770047), H2020 WASP (Contract No. 50 825213), and the Graphene Flagship Core3 (Contract No. 881603). R.W. acknowledges the Hewlett-Packard Company for financial support in the framework of the Graphene NOWNANO Centre for Doctoral Training.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

Research data are not shared.

Keywords

1/f noise, 2D materials, inkjet-printing, MoS₂ transistors, paper electronics

Received: March 19, 2021

Published online: May 29, 2021

- [1] T. Yokota, P. Zalar, M. Kaltenbrunner, H. Jinno, N. Matsuhsa, H. Kitano, Y. Tachibana, W. Yukita, M. Koizumi, T. Someya, *Sci. Adv.* **2016**, *2*, e1501856.
- [2] G. A. Salvatore, N. Münzenrieder, T. Kinkeldei, L. Petti, C. Zysset, I. Strelbel, L. Büthe, G. Tröster, *Nat. Commun.* **2014**, *5*, 2982.
- [3] L. Petti, N. Münzenrieder, C. Vogt, H. Faber, L. Büthe, G. Cantarella, F. Bottacchi, T. D. Anthopoulos, G. Tröster, *Appl. Phys. Rev.* **2016**, *3*, 021303.
- [4] B. C.-K. Tee, A. Chortos, A. Berndt, A. K. Nguyen, A. Tom, A. McGuire, Z. C. Lin, K. Tien, W.-G. Bae, H. Wang, P. Mei, H.-H. Chou, B. Cui, K. Deisseroth, T. N. Ng, Z. Bao, *Science* **2015**, *350*, 313.
- [5] M. Stoppa, A. Chiolerio, *Sensors* **2014**, *14*, 11957.
- [6] S. Manzeli, D. Ovchinnikov, D. Pasquier, O. V. Yazyev, A. Kis, *Nat. Rev. Mater.* **2017**, *2*, 17033.
- [7] J. Pu, Y. Yomogida, K.-K. Liu, L.-J. Li, Y. Iwasa, T. Takenobu, *Nano Lett.* **2012**, *12*, 4013.
- [8] R. Cheng, S. Jiang, Y. Chen, Y. Liu, N. Weiss, H.-C. Cheng, H. Wu, Y. Huang, X. Duan, *Nat. Commun.* **2014**, *5*, 5143.
- [9] H.-Y. Chang, S. Yang, J. Lee, L. Tao, W.-S. Hwang, D. Jena, N. Lu, D. Akinwande, *ACS Nano* **2013**, *7*, 5446.
- [10] W. G. Song, H.-J. Kwon, J. Park, J. Yeo, M. Kim, S. Park, S. Yun, K.-U. Kyung, C. P. Grigoropoulos, S. Kim, Y. K. Hong, *Adv. Funct. Mater.* **2016**, *26*, 2426.
- [11] Q. He, Z. Zeng, Z. Yin, H. Li, S. Wu, X. Huang, H. Zhang, *Small* **2012**, *8*, 2994.
- [12] J. Yoon, W. Park, G.-Y. Bae, Y. Kim, H. S. Jang, Y. Hyun, S. K. Lim, Y. H. Kahng, W.-K. Hong, B. H. Lee, H. C. Ko, *Small* **2013**, *9*, 3295.
- [13] M. Choi, Y. J. Park, B. K. Sharma, S. Bae, S. Y. Kim, J. Ahn, *Sci. Adv.* **2018**, *4*, eaas8721.
- [14] M.-Y. Tsai, A. Tarasov, Z. R. Hesabi, H. Taghinejad, P. M. Campbell, C. A. Joiner, A. Adibi, E. M. Vogel, *ACS Appl. Mater. Interfaces* **2015**, *7*, 12850.
- [15] G.-H. Lee, Y. Yu, X. Cui, N. Petrone, C.-H. Lee, M. S. Choi, D.-Y. Lee, C. Lee, W. J. Yoo, K. Watanabe, T. Taniguchi, C. Nuckolls, P. Kim, J. Hone, *ACS Nano* **2013**, *7*, 7931.
- [16] B. Sirota, N. Glavin, A. A. Voevodin, *Vacuum* **2019**, *160*, 133.
- [17] M. Irimia-Vladu, *Chem. Soc. Rev.* **2014**, *43*, 588.
- [18] D. Tobjörk, R. Österbacka, *Adv. Mater.* **2011**, *23*, 1935.
- [19] Available at: <https://irds.ieee.org/editions/2020> (accessed: July 2020).
- [20] P. Sahatiya, S. Badhulika, *Adv. Electron. Mater.* **2018**, *4*, 1700388.
- [21] S. Conti, L. Pimpolari, G. Calabrese, R. Worsley, S. Majee, D. K. Polyushkin, M. Paur, S. Pace, D. H. Keum, F. Fabbri, G. Iannaccone, M. Macucci, C. Coletti, T. Mueller, C. Casiraghi, G. Fiori, *Nat. Commun.* **2020**, *11*, 3566.
- [22] A. A. Balandin, *Nat. Nanotechnol.* **2013**, *8*, 549.
- [23] F. Gasparyan, H. Khondkaryan, A. Arakelyan, I. Zadorozhnyi, S. Pud, S. Vitusevic, *J. Appl. Phys.* **2016**, *120*, 064902.
- [24] V. K. Sangwan, H. N. Arnold, D. Jariwala, T. J. Marks, L. J. Lauhon, M. C. Hersam, *Nano Lett.* **2013**, *13*, 4351.
- [25] H. J. Kwon, H. Kang, J. Jang, S. Kim, C. P. Grigoropoulos, *Appl. Phys. Lett.* **2014**, *104*, 083110.
- [26] S. L. Rumyantsev, C. Jiang, R. Samnakay, M. S. Shur, A. A. Balandin, *IEEE Electron Device Lett.* **2015**, *36*, 517.
- [27] D. Sharma, M. Amani, A. Motayed, P. B. Shah, A. G. Birdwell, S. Najmaei, P. M. Ajayan, J. Lou, M. Dubey, Q. Li, A. V. Davydov, *Nanotechnology* **2014**, *25*, 155702.
- [28] Y. Wang, X. Luo, N. Zhang, M. R. Laskar, L. Ma, Y. Wu, S. Rajan, W. Lu, *82nd ARFTG Microw. Meas. Conf. Charact. Model. Des. RF mm-Wave Devices Circuits, ARFTG* **2013**, *2013*, 2.
- [29] N. Kaushik, S. Ghosh, S. Lodha, *IEEE Trans. Electron Devices* **2018**, *65*, 4135.
- [30] J. W. Wang, Y. P. Liu, P. H. Chen, M. H. Chuang, A. Pezeshki, D. C. Ling, J. C. Chen, Y. F. Chen, Y. H. Lee, *Adv. Electron. Mater.* **2018**, *4*, 1.
- [31] J. Na, M. Joo, M. Shin, J. Huh, J. Kim, M. Piao, J.-E. Jin, H.-K. Jang, H. J. Choi, J. H. Shim, G.-T. Kim, *Nanoscale* **2014**, *6*, 433.
- [32] C. A. Schneider, W. S. Rasband, K. W. Eliceiri, *Nat. Methods* **2012**, *9*, 671.
- [33] D. McManus, S. Vranic, F. Withers, V. Sanchez-romaguera, M. Macucci, H. Yang, R. Sorrentino, K. Parvez, S. Son, G. Iannaccone, K. Kostarelos, G. Fiori, C. Casiraghi, *Nat. Nanotechnol.* **2017**, *12*, 343.
- [34] R. Worsley, L. Pimpolari, D. Mcmanus, N. Ge, R. Ionescu, J. A. Wittkopf, A. Alieva, G. Basso, M. Macucci, G. Iannaccone, K. S. Novoselov, H. Holder, G. Fiori, C. Casiraghi, *ACS Nano* **2019**, *13*, 56.
- [35] P. Karnatak, T. Paul, S. Islam, A. Ghosh, *Adv. Phys. X* **2017**, *6149*, 211.
- [36] G. Calabrese, L. Pimpolari, S. Conti, F. Mavie, S. Majee, R. Worsley, Z. Wang, F. Pieri, G. Basso, G. Pennelli, K. Parvez, D. Brooks, M. Macucci, G. Iannaccone, K. S. Novoselov, C. Casiraghi, G. Fiori, *Nanoscale* **2020**, *12*, 6708.
- [37] S. Das, H. Chen, A. V. Penumatcha, J. Appenzeller, *Nano Lett.* **2013**, *13*, 100.
- [38] C. Kim, I. Moon, D. Lee, M. S. Choi, F. Ahmed, S. Nam, Y. Cho, H. Shin, S. Park, W. J. Yoo, *ACS Nano* **2017**, *11*, 1588.
- [39] B. Stampfer, F. Zhang, Y. Y. Illarionov, T. Knobloch, P. Wu, M. Waltl, A. Grill, J. Appenzeller, T. Grasser, *ACS Nano* **2018**, *12*, 5368.
- [40] F. N. Hooge, *Phys. Lett. A* **1969**, *29*, 139.
- [41] A. Behranginia, P. Yasaei, A. K. Majee, V. K. Sangwan, F. Long, C. J. Foss, T. Foroozan, S. Fuladi, M. R. Hantehzadeh, R. Shahbazian-Yassar, M. C. Hersam, Z. Aksamija, A. Salehi-Khojin, *Small* **2017**, *13*, 1604301.
- [42] J. Kim, Y. Song, T. Kim, K. Cho, J. Park, B. Y. Choi, J. Shin, S. Chung, T. Lee, *Nanotechnology* **2017**, *28*, 47LT01.
- [43] S. Das, J. Kwon, D. Janes, *Mater. Res. Soc. Symp. Proc.* **2014**, *723*, 1701.
- [44] X. Xie, D. Sarkar, W. Liu, J. Kang, O. Marinov, J. Deen, K. Banerjee, *ACS Nano* **2014**, *8*, 5633.
- [45] D. Sharma, A. Motayed, P. B. Shah, M. Amani, M. Georgieva, A. G. Birdwell, Q. Li, A. V. Davydov, *Appl. Phys. Lett.* **2015**, *107*, 162102.
- [46] W. Zeng, L. Shu, Q. Li, S. Chen, F. Wang, X. M. Tao, *Adv. Mater.* **2014**, *26*, 5310.